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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,414	10/02/2000	David W. Carlson	NSC1-H1700 [P04797]	4381

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,414	CARLSON, DAVID W.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Claims 31 - 52 are now pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 31-36, 38, 39, 42-47, 49 and 50 are rejected under 35 U.S.C. 102(e) as being anticipate by Li et al. (US/6,162,368).

The rejection that was mailed on December 16, 2005 is maintained and repeated herein below as of record.

Re claims 31 and 42, Li et al. disclose a method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising: forming a layer of first material (16) to contact the top surface of the wafer (10), the layer of first material (16) having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level; forming a layer of second material (18) to contact the top surface of the layer of first material (16), the layer of second material being non-planar to

surface; and chemically-mechanically polishing the non-planar top surface of the layer of second material (18) and the underlying layer of first material (16) with a slurry to form the planarized layer of second material (see Figs. 2D-2F); and wherein the layer of first material makes an electrical contact with a device on the wafer, the planarized layer of material lying over the wafer upper levels and the wafer lower level, the layer of the first material (16) having substantially planar top surface when the layer of second material (18) as soon as substantially all removed (see Fig. 2D) form the layer of first material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 32, as applied to claim 31 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material has first thickness over the wafer upper level and, wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claims 33 - 35, as applied to claim 31 above, Li et al. disclose all the claimed limitations including the limitation wherein the layer of first material is conductive layer (i.e., doped polysilicon which is doped prior forming the second material) and electrically connected to the device on wafer (i.e., substrate) (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 36, as applied to claim 31 above, Li et al. disclose all the claimed limitations including the limitation the second material is non-conductive (i.e., being an oxide) (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 38 and 39, as applied to claim 31 above, Li et al. disclose all the claimed limitations including forming a layer of third material (i.e., also mask layer) on the planarized layer of material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 43, as applied to claim 42 above, Li et al. disclose all the claimed limitations including the limitation wherein the planarized layer of material has first thickness over the wafer upper level and, wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a second thickness that is equal to or greater than the first thickness (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claims 44 - 47, as applied to claim 42 above, Li et al. disclose all the claimed limitations including the limitation wherein the layer of first material is conductive layer (i.e., doped polysilicon which is doped prior forming the second material) and electrically connected to the device on wafer and the second material is non-conductive (i.e., substrate) (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Re claim 49 and 50, as applied to claim 42 above, Li et al. disclose all the claimed limitations including forming a layer of third material (i.e., also mask layer) on the planarized layer of material (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 37 and 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US/6,162,368), as applied in Paragraph 3 above, in view of Weling et al. (US/5,378,318).

The rejection that was mailed on December 16, 2005 is maintained and repeated herein below as of record.

Re claims 37 and 48, as applied to claims 31 and 42 in Paragraph 3 above, Li et al. disclose all the claimed limitations including using CMP process with a slurry that has a predetermined etch rate.

However, Li et al. do not specifically disclose the etch selectivity of the first material to the second material approximately same rate (i.e., being 0.9-1.1:1).

Weling et al. disclose CMP of the first material (21) and second material (23) with a eth selectivity of 1:1, (i.e., approximately same rate) (see Fig. 1, Col. 7, lines 6-11).

Both Li et al. and Weling et al. teachings are directed to CMP process in order to planarize a material for semiconductor device fabrication. Therefore, the teachings Li et al. and Weling et al. are analogous

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Li et al. reference with etch selectivity ratio 1:1 as taught by Weling et al. because in order to polish the first layer and second layer at the same rate and form planar surface for the fabrication of semiconductor device.

6. **Claims 40, 41, 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US/6,162,368), as applied in Paragraph 3 above, in view of Sandhu et al. (US/5,381,302).**

A new ground of rejection is set froth below.

Re claims 40 and 51, as applied to claims 38 and 49 respectively in Paragraph 3 above, Li et al. disclose all the claimed limitations including the planarized layer of material includes doped polysilicon.

Although it is well-known in the art to deposit metallic layer that forms silicide sheet resistance of the polysilicon layer, Li et al. do not specifically disclose that layer of third material lowers a resistance of doped polysilicon (see Figs. 2A-2I and Col. 4, line 37 through Col. 6, line 54).

Sandhu et al. disclose a method of fabricating a semiconductor device the method includes forming a doped polysilicon (65) in the opening (50) and polishing of the doped polysilicon (65) (see Figs. 4 and 5) and forming metallic layer (62) (i.e., Ti layer that lowers resistance of the doped polysilicon layer) in order to form titanium silicide layer (67) (see Fig. 7 and related text in Col. 5, line 10 -67) that lowers the sheet resistance of the polysilicon layer.

Both Li et al. and Sandhu et al. teachings are directed to CMP process in order to planarize a polysilicon material for semiconductor device fabrication. Therefore, the teachings Li et al. and Sandhu et al. are analogous

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Li et al. reference with depositing of Ti based material layer over the doped polysilicon layer Sandhu et al because titanium is a known material in the art reducing the sheet resistance of the doped polysilicon layer by silicidation process.

Re claims 41 and 52, as applied to claims 40 and 51 above, Li et al. and Sandhu et al. in combination disclose all the claimed limitations including forming a mask on the layer of third

material (i.e., Sandhu et al. use the mask by keeping the titanium over the polysilicon plug while removing the titanium layer on the portion the ILD layer, as depicted on Fig. 8).

Response to Arguments

7. Applicant's arguments with respect to claims 51 and 52 have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's arguments filed on March 20, 2006 have been fully considered but they are not persuasive.

Applicant further argued that "As shown Fig. 2C, Ki teaches that as soon as native oxide layer 18, *the second material*, has been removed, polysilicon 16, the first material, does not have substantially planar top surface as required by claims..."

In response to the applicant's argument, it is respectfully submitted that Li et al. '368 disclose all the claimed limitations the instant application as claimed in claims 31-36, 38-46 and 49-52 as applied above. For example, as shown in Fig. 2D and presented herein below, the first material layer **16** does actually polished to have planar surface prior layer **50b , 106** and **104** are deposited. The removal of the second material layer 18 and planarizing of the second material 16 is happened concurrently within short period of time by CMP process (see also Col. 6, lines 1-5).

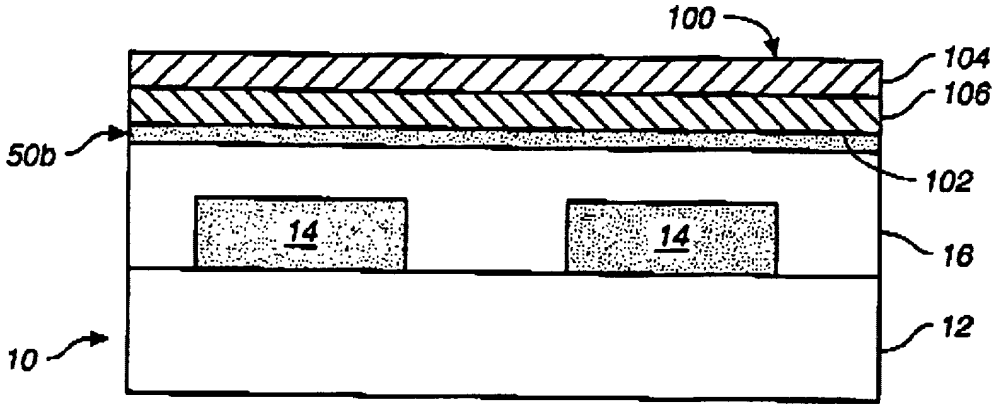

FIG._2D

After the CMP process and removal of the material layer **18**, the first material layer **16** having a substantially planar surface **19** as shown in Fig. 2G herein below.

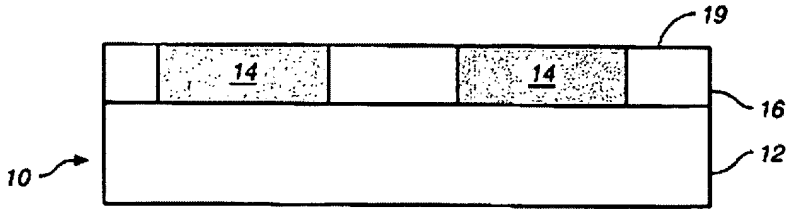

FIG._2G

Further in response to applicant's contention, it is respectfully submitted the instant application claimed invention does not specifically disclose to the degree of certainty that instant application CMP process will result a perfect planar surface that cannot be achieved by the CMP process of Li et al. '368. There is no evidence can be found in the instant application to the contrary of Li et al. '368 disclosure.

Applicant further argues that "Li fails to teach or suggest formation of third material as claimed ..."

In repose to applicant's argument, it is respectfully submitted that Li et al. '368 disclose all the claimed limitations of the instant application as claimed including forming of third material over the planarized second material **16**. For example, Fig. 2I as shown below material layer **114** is meets the claim language third material layer as applied in the rejected claims in Paragraph 4 above.

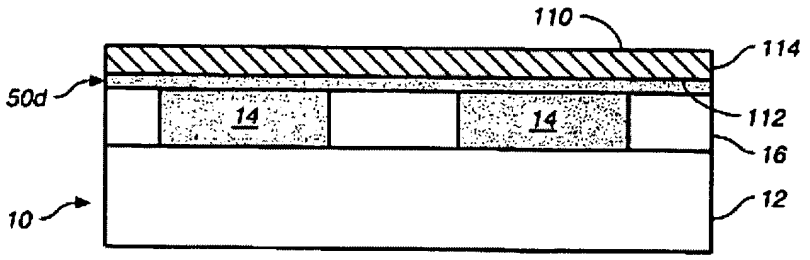

FIG._2I

Further in response to applicants contention that "*Li does not teach or suggest* wherein the third layer is a mask *layer* ...," it is respectfully submitted that "mask" layer does not have any special meaning as claimed in claims 39 and 50 because applicant does not define what the mask layer entails or represent in terms of it function and usage. Since "mask" has a very broad interpretation and function in the semiconductor industry, the "pad" layer is analogous to "mask" for CMP process. If applicant can provide an evidence the function of "mask" in the instant application different form "pad" in Li et al. the Office would like to see such evidence and such evidence will be valuable in determining of patentability of the instant application. In absence of clear definition to the function and/or meaning of "mask" in the instant application, it is interpreted that Li et al.'s "pad" layer meets the scope and meaning of "mask".

"*See In re Paulsen*, 30 F.3d 1475, 1480, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994). inventor may define specific terms used to describe invention, but must do so "**with reasonable clarity, deliberateness, and precision" and, if done, must "set out his uncommon definition in some manner within the patent disclosure**' so as to give one of ordinary skill in the art notice of the change" in meaning) (*quoting Intellicall, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384, 1387-88, 21 USPQ2d 1383, 1386 (Fed. Cir. 992)). Any special meaning assigned to a term "must be sufficiently clear in the specification that any departure from common usage would be so understood by a person of experience in the field of the invention." *Multiform Desiccants Inc. v. Medzam Ltd.*, 133 F.3d 1473, 1477, 45 USPQ2d 1429, 1432 (Fed. Cir. 1998). See also Process *Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999)."

Furthermore, the rejected claims do not specifically claim the type of material and process step such a way can be distinguishable form Li et al. '368 disclosure. In this regard, claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

As shown above, the rejection under 35 U.S.C. §102(e) is deemed proper and the rejection under 35 U.S.C. §103(a) also deemed proper and the *prima facie* case of obviousness has been met.

Conclusion

9. **THIS ACTION IS MADE NON-FINAL.**

Correspondence

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede

Brook Kebede
Primary Examiner
Art Unit 2823

BK
May 23, 2006